High-performance BiCMOS Current Controlled CDBA and application

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Abstract- This article presents the modified design for a basic current-mode building block for analog signal processing, named as current controlled current differencing buffered amplifier (CCCDBA). Its parasitic resistances at two current input ports can be controlled by an input bias current. The output current and voltage offsets including power consumption are low compared to ordinary CCCDBA description with same implemented technology. The proposed element is realized in a BiCMOS technology and its performance is examined through PSPICE simulations. In addition, an example as a current-mode multiplier/divider is included. It displays usability of the proposed element.

I. INTRODUCTION

In the last decade, there has been much effort to reduce the supply voltage of electronic circuits. This is due to the demand for portable and battery-powered equipment. Since a low-voltage operating circuit becomes necessary, the current-mode technique is ideally suited for this purpose more than the voltage-mode one. Consequently, there is a growing interest in synthesizing the current-mode circuits because of more their potential advantages such as larger dynamic range, higher signal bandwidth, greater linearity, simpler circuitry and lower power consumption [1-2]. Many active elements able to function in current-mode such as OTA, current conveyor, current differencing buffered amplifier (CDBA) and current differencing transconducance amplifier (CDTA), have been introduced to response these demands.

The current differencing buffered amplifier is a reported active component especially suitable for a class of analog signal processing [3]. The fact that the device can operate in both current and voltage-modes, provides flexibility and enables a variety of circuit designs. In addition, it can offer advantageous features such as high-slew rate, free from parasitic capacitances, wide bandwidth and simple implementation [4]. However, the CDBA can not be controlled by the parasitic resistances at two current input ports so when it is used in some circuits, it must unavoidably require some external passive components, especially the resistors. This makes it not appropriate for IC implementation due to occupying more chip area, high power dissipation and without electronic controllability. Recently, Maheshwari and Khan have proposed the modified-version CDBA whose the parasitic resistances at two current input ports can be controlled by an input bias current and it is newly named current controlled current differencing buffered amplifier (CCCDBA) [5]. Since the CCCDBA in [5] was implemented by using a BJT technology. Unfortunately, this structure has problems of the offset output levels and high power consumption because it uses the BJTs to implement the current mirrors.

The purpose of this paper is to design and synthesize a modified-version CCCDBA in a BiCMOS technology to reduce the offset output levels and power consumption. The translinear properties of BJTs are still used in proposed element, while the CMOSs are used to implement the current mirrors instead of the BJTs. In addition, a new voltage buffer is employed to obtain less output offset voltage. The performances of proposed BiCMOS CCCDBA are illustrated by PSPICE simulations, they show good agreement as mentioned. An example application as a multiplier/divider is comprised.

Figure 1. The CCCDBA (a) Symbol (b) Equivalent Circuit

II. CIRCUIT CONFIGURATION

A. Basic Concept of CCCDBA

CCCDBA properties are similar to the conventional CDBA, except that input voltages of CCCDBA are not zero and the CCCDBA has finite input resistances \( R_p \) and \( R_n \) at the \( p \) and \( n \) input terminals, respectively. These parasitic resistances are equal and can be controlled by the bias current \( I_b \) by

\[
\begin{bmatrix}
V_p \\
V_n \\
I_n \\
V_i \\
I_v
\end{bmatrix} =
\begin{bmatrix}
R_p & 0 & 0 & 0 & I_v \\
0 & R_n & 0 & 0 & I_v \\
1 & -1 & 0 & 0 & V_i \\
0 & 0 & 1 & 0 & I_v
\end{bmatrix}
\begin{bmatrix}
I_p \\
I_n \\
1 \\
0 \\
0
\end{bmatrix}.
\]
A. The aspect transistor ratios

\[ R_y = R_e = \frac{V_t}{2I_b}, \]  
where \( V_t \) is the thermal voltage. The symbol and the equivalent circuit of the CCCDBA are illustrated in Fig. 1(a) and (b), respectively.

B. Proposed BiCMOS Current Controlled Current Differencing Buffered Amplifier

The proposed CCCDBA consists of two principal blocks: a current differencing circuit which has finite input resistances and a voltage buffer circuit [5]. The proposed realization of the CCCDBA in a BiCMOS configuration is shown in Fig. 2. The circuit implementation consists of mixed translinear loops (\( Q_1-Q_3 \)). The mixed loops are DC biased by \( I_b \) using current mirrors (\( M_4-M_7 \) and \( M_6-M_7 \)). The \( p \) and \( n \) resistances can be obtained by Eq. (2). The output \( z \) terminal that generates the current difference of \( p \) and \( n \) terminals is realized using CMOSs (\( M_2-M_5 \) and \( M_9-M_{12} \)). The buffered amplifier is realized using BJTs and CMOSs (\( Q_9-Q_{21} \) and \( M_{14}-M_{21} \)) [6].

The output resistances looking into the \( z \) and \( w \) terminals can be respectively expressed as

\[ r_z = \frac{r_d}{2}, \]

and

\[ r_w = \frac{r_c}{4} \beta r_A. \]

where \( r_d \) is the drain-source resistance and \( r_c \) is the collector-emitter resistance seen at the mentioned output terminals.

III. Simulation Results

To prove the performances of the proposed CCCDBA, the PSPICE simulation program was used for the examinations. The PNP and NPN transistors employed in the proposed circuit in Fig. 2 were simulated by respectively using the parameters of the PR200N and NR200N bipolar transistors of ALA400 transistor array from AT&T [7]. The PMOS and NMOS transistors were simulated by using the parameters of a 0.35\( \mu \)m TSMC CMOS technology [8] with \( \pm 1.5 \)V supply voltages and \( I_D \) was set to 150 \( \mu \)A. The aspect transistor ratios of PMOS and NMOS are listed in Table I. Fig. 3 depicts the parasitic resistances at \( p \) and \( n \) input terminals when \( I_b \) was varied, it is seen that the controllable parasitic resistances by adjusting \( I_b \) is in 1\( \mu \)A-180\( \mu \)A range.

TABLE I

<table>
<thead>
<tr>
<th>CMOS Transistors</th>
<th>( W(\mu m) \times L(\mu m) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M5, M14-M17, M18-M19</td>
<td>5/0.5</td>
</tr>
<tr>
<td>M6-M7</td>
<td>20/0.5</td>
</tr>
<tr>
<td>M8-M11</td>
<td>15/0.5</td>
</tr>
<tr>
<td>M12-M13</td>
<td>20/0.5</td>
</tr>
<tr>
<td>M20-M21</td>
<td>100/5</td>
</tr>
</tbody>
</table>

Fig. 4 displays DC transfer characteristics of the proposed BiCMOS CCCDBA, where \( I_b = 100 \mu A \). So it is seen that they are linear in \(-100 \mu A \leq I_b \leq 100 \mu A\) and can be adjusted. Fig. 5 shows comparison of the offset current variations obtained from element in [5] and from our proposed element which respects to the input bias current \( I_b \) when \( I_a \) and \( I_b \) are equal. It is seen that the proposed BiCMOS CCCDBA provides much lower current offset. Fig. 6 shows DC variations at output terminal for the element in [5] and our proposed element. It is also seen that our proposed element

![Figure 2: Proposed BiCMOS current controlled current differencing buffered amplifier](image)

![Figure 3: Parasitic resistances at input terminals relative to \( I_b \)](image)

![Figure 4: DC transfer characteristics of proposed BiCMOS CCCDBA](image)
provides lower output offset voltage. The power consumptions of the CCCDBA in [5] and proposed are 1.39mW and 655μW, respectively. The summarized parameters of the proposed CCCDBA can be seen in Table II.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumption</td>
<td>655 μW</td>
</tr>
<tr>
<td>-3 dB Bandwidth</td>
<td>28.54 MHz ({I_n}/{I_p})</td>
</tr>
<tr>
<td></td>
<td>33.48 MHz, ({I_n}/{I_p})</td>
</tr>
<tr>
<td></td>
<td>257.82 MHz, (V_w/V_z)</td>
</tr>
<tr>
<td>Input current linear range</td>
<td>100 μA to 100 μA</td>
</tr>
<tr>
<td>R_n and R_p ranges</td>
<td>223.29 kΩ-6.27 kΩ</td>
</tr>
<tr>
<td>Input bias current range</td>
<td>1 μA-180 μA</td>
</tr>
<tr>
<td>for controlling R_n and R_p</td>
<td></td>
</tr>
</tbody>
</table>

![Figure 5. Variations of the output offset current](image)

![Figure 6. DC variations of output voltage at w terminal](image)

**TABLE II**

**CONCLUSIONS OF CCCDBA PARAMETERS**

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IV. APPLICATION EXAMPLE AS A CURRENT-MODE MULTIPLIER/DIVIDER

The multiplier/divider based on the CCCDBAs is shown in Fig. 7. It consumes few amounts of active elements compared to ordinarily proposed circuits [9-10], employing only two CCCDBAs. From routine analysis and using the CCCDBA properties, we will receive the output current by

\[ I_o = \frac{V_{w2}}{R_{v2}} = I_a \frac{R_{g1}}{2R_{g2}} \]  

(5)

If \( R_{g1} = V_i / 2I_p \) and \( R_{g2} = V_i / 2I_c \). The output current in Eq. (5) will be changed to

\[ I_o = \frac{I_c}{2I_b} \]  

(6)

From Eq. (6), it is seen that \( I_o \) is a result of either, multiplying of \( I_a \) and \( I_c \), or dividing of \( I_a \) and \( I_b \). Due to being a positive value of \( I_b \) and \( I_c \), the proposed circuit can be a 2 quadrant multiplier/divider. In addition, if \( I_a \) is an input current, the proposed circuit can work as a current amplifier, which the magnitude of output current can be controlled by \( I_b \) and \( I_c \).

![Figure 7. Multiplier/divider based on the CCCDBAs](image)

![Figure 8. Static characteristics of multiplication](image)

![Figure 9. Static characteristics of division](image)

Fig. 8 shows compared results for the DC characteristics of multiplication obtained from the circuit implemented from the element in [5] and that from our proposed element, where \( I_b=40μA \). Fig. 9 shows compared results for the DC characteristics of division obtained from the circuit implemented from the element in [5] and that from our proposed element, where \( I_c=20μA \). There can be concluded that the circuit realized from our proposed element offers lower offset levels.

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The analog building block, called BiCMOS CCCDBA, has been introduced. The usabilities have been proven by the simulation and application examples. The proposed element provides electronic controllability, low output offsets including low power consumption. Thus, it is very appropriate to realize in commercially-purposed integrated circuit to be employed in battery-powered, portable electronic equipments or wireless communication systems. Our future work is to present more useable applications of this element such as filter, precision rectifier, etc.

Fig. 11. Output current deviations due to temperature variations of the proposed circuit as (a) Multiplier (b) Divider

Fig. 12. Output currents relative to different Ic

Conclusions

REFERENCES


Ic=Iin=40μA. The maximum bandwidth of the output current of 26.42MHz, is shown in Fig. 13.