A Simple Temperature-insensitive, Electronically Controllable Floating Capacitance Multiplier

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Abstract

This article introduces a floating capacitance multiplier employing differential voltage current conveyor (DVCC) and current control current conveyor transconductance amplifier (CCCCTA). The provided capacitor is a floating element synthesized from a grounded capacitor. Its outstanding feature is that the capacitive value can be electronically adjusted by input bias currents of the CCCCTA and is temperature-insensitive. The circuit construction comprises only one DVCC and one CCCCTA, cooperating with a grounded capacitor. The circuit performances are depicted through PSPICE simulations, they show good agreement to theoretical anticipation. Capacitance increasing and an application as a fifth-order Chebyshev high-pass filter are included.

Keywords: CCCCTA, Capacitance multiplier

1. Introduction

It is well accepted that a capacitor is an important element which is frequently used in the most of circuits and systems. For example, it is used for tuning in filters, oscillators and etc. However, in the integrated circuit fabrication, it is impractical to realize large-valued capacitors because of the occupied area. In fact, in a standard CMOS polysilicon layers, a 20pF capacitor is equivalent, relatively to the silicon area, to thousands of transistors [1]. This means that the integration of capacitor as large as 100pF is not possible. In some applications, however, such as integrated lock-in amplifiers, sampled-data systems and capacitive sensor interfaces [2-5], they are necessary to have higher capacitive values.

A possible solution is the use of a capacitance multiplier, which performs the multiplication of small capacitive values, to obtain higher equivalent integrated capacitors, avoiding the need of a large silicon area [6]. From literature studies, several works which can provide a multiplied capacitor have been
Figure 8 Phase and Magnitude of input impedance relative to frequency variations

Figure 9 Frequency responses of magnitude of input impedance due to temperature variations

Figure 10 Magnitude of input impedance relative to frequency variations of circuit in Figure 4 for different current gains where the ideal current amplifier is used for the simulation. It should be noted here that the synthesized capacitive value can be tuned by the current gain \( n \), which is accordant to Eq. (10). The floating capacitance multiplier in the cited references [19] and the configuration proposed in this paper are compared in Table 2.

To show usability of the proposed capacitor multiplier, an application of the synthesized capacitor in a fifth-order Chebyshev high-pass filter [25] as shown in Figure 11 is included. The results of frequency responses of the filter implemented by the proposed capacitance multiplier, compared to those by ideal capacitors, are confirmed in Figure 12, where \( V_m = 2mV \).

Table 2 Comparison of the floating capacitance multiplier in the literature [19] and proposed topology in this paper

<table>
<thead>
<tr>
<th>Proposed circuit</th>
<th>Reference [19]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>±1.5V</td>
</tr>
<tr>
<td>±2.5V</td>
<td></td>
</tr>
<tr>
<td>Power consumption</td>
<td>321( \mu )W</td>
</tr>
<tr>
<td>7.32mW</td>
<td></td>
</tr>
<tr>
<td>Amount of Active elements</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
</tbody>
</table>

In addition, from the result in Figure 9, it is insisted that in the usable frequency range, the proposed circuit provides a floating capacitance with temperature-insensitivities.
Table 1 displays capacitance deviations of obtained capacitances due to capacitance and multiplied gain variations.

Figure 8 shows the phase and magnitude of input impedance for frequency variations. It should be noted that the usable frequency range of the proposed circuit is up to approximately MHz range.

![Figure 7 Transient responses of current and voltage dropping input of capacitance multiplier](image)

Table 1. Capacitance deviations of obtain Capacitance at several Capacitor and multiplied gain

<table>
<thead>
<tr>
<th>Multiplied Gain</th>
<th>Capacitors (pF)</th>
<th>Obtained Capacitance (pF)</th>
<th>Errors (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10</td>
<td>10.1</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>10</td>
<td>51.5</td>
<td>2.91</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>103.8</td>
<td>3.8</td>
</tr>
<tr>
<td>20</td>
<td>10</td>
<td>207.3</td>
<td>3.65</td>
</tr>
<tr>
<td>30</td>
<td>10</td>
<td>303.15</td>
<td>1.05</td>
</tr>
<tr>
<td>40</td>
<td>10</td>
<td>411.8</td>
<td>2.95</td>
</tr>
<tr>
<td>50</td>
<td>10</td>
<td>517.03</td>
<td>3.41</td>
</tr>
<tr>
<td>60</td>
<td>10</td>
<td>624.13</td>
<td>4.02</td>
</tr>
<tr>
<td>70</td>
<td>10</td>
<td>730.73</td>
<td>4.39</td>
</tr>
<tr>
<td>80</td>
<td>10</td>
<td>840.2</td>
<td>5.03</td>
</tr>
<tr>
<td>90</td>
<td>10</td>
<td>951.42</td>
<td>5.71</td>
</tr>
<tr>
<td>100</td>
<td>10</td>
<td>1061.03</td>
<td>6.1</td>
</tr>
</tbody>
</table>
3. Design Methodology
3.1 Proposed Capacitance Multiplier

Figure 3 depicts the proposed floating capacitance multiplier. Considering the circuit in Figure 3 and using DVCC and CCCCTA properties in section 2.1 and 2.2, we will receive

$$Z_m = \frac{V_i - V_x}{I_m} = \frac{2}{g_m R_x C s}.$$  \hspace{1cm} (5)

From Eq. (5), it is clearly seen that, the proposed circuit can provide the new floating capacitor with a value

$$C_k = \frac{g_m R_x C}{2}.$$ \hspace{1cm} (6)

If we substitute $R_x = V_r / 2I_{b1}$ and $g_m = I_{g1} / 2V_r$, the floating capacitance is modified to

$$C_k = K_{mul} C = \frac{I_{g2}}{8I_{g1}} C.$$ \hspace{1cm} (7)

It is evident that, the capacitive value is multiplied with a gain as

$$K_{mul} = \frac{I_{g2}}{8I_{g1}}.$$ \hspace{1cm} (8)

We can found that, if the connected capacitor is ideally free from temperature variations, the obtained capacitive value from the proposed circuit is temperature-insensitive and can be adjusted by any input bias currents $I_c$.

3.2 Principle of capacitance increasing

Figure 4 gives the theoretical implementation of the high-value capacitance controllabilities. The output stage of circuit in Figure 4 is constituted by a dual output-current amplifier. Then, the output currents of current amplifier are equal to $I_o = nI_o$. Thus, the input impedance of circuit in Figure 4 becomes

$$Z_m = \frac{V_i - V_x}{I_c} = \frac{2}{n g_m R_x C s}.$$ \hspace{1cm} (9)

It is evident that, the capacitive value is multiplied with a gain

$$K_{mul} = \frac{n I_{g2}}{8I_{g1}}.$$ \hspace{1cm} (10)

From Eq. (10), it is clearly seen that, we can control the capacitive value by adjusting the current gain $(n)$ of the current amplifier circuit.
consumption. The performances of proposed circuit are illustrated by PSPICE simulations, they show good agreement as depicted. Capacitance increasing and an application as a fifth-order Chebyshev high-pass filter are included.

2. Principle of Operation

2.1 Differential Voltage Current Conveyor (DVCC)

The DVCC, whose electrical symbol and equivalent circuit are shown in Figure 1, is a four-terminal network with the terminal ideal characteristics are described by following equation

\[
\begin{bmatrix}
V_x \\
I_{x1} \\
I_{x2} \\
I_x
\end{bmatrix} = \begin{bmatrix}
0 & 1 & -1 & 0 \\
0 & 0 & 0 & V_{x1} \\
0 & 0 & 0 & V_{x2} \\
1 & 0 & 0 & 0
\end{bmatrix} \begin{bmatrix}
I_x \\
V_{x1} \\
V_{x2} \\
V_x
\end{bmatrix}
\]  

(1)

![Figure 1 The DVCC symbol](image)

![Figure 1 The DVCC equivalent circuit](image)

2.2 Current Controlled Current Conveyor

Transconductance Amplifier (CCCCTA)

CCCCTA properties are similar to the conventional CFTA [23], except that the CCCCTA has finite input resistance \( R_x \) at the \( x \) input terminal. This parasitic resistance can be controlled by the bias current \( I_{B1} \) as shown in the following equation

\[
\begin{bmatrix}
I_x \\
V_x \\
I_x \\
I_v
\end{bmatrix} = \begin{bmatrix}
0 & 0 & 0 & 0 \\
R_x & 0 & 0 & V_x \\
1 & 0 & 0 & 0 \\
0 & 0 & \pm g_m & 0
\end{bmatrix} \begin{bmatrix}
I_x \\
V_x \\
V_x \\
V_x
\end{bmatrix}
\]  

(2)

where

\[
R_x = \frac{V_T}{2I_{B1}}
\]  

(3)

and

\[
g_m = \frac{I_{B2}}{2V_T}
\]  

(4)

where \( g_m \) is the transconductance gain of the CCCCTA and \( V_T \) is the thermal voltage. The symbol and equivalent circuit of the CCCCTA are illustrated in Figure 2(a) and (b), respectively

![Figure 2 The CCCCTA symbol](image)

![Figure 2 The CCCCTA equivalent circuit](image)
proposed. Although, the voltage-mode operational amplifier (op-amp) based capacitance multipliers are available in the literatures [7-9], they are not suitable from the view point of IC fabrication.

The modern active building blocks employed to synthesize the capacitance multipliers, emphasized on Operational Transconductance Amplifiers (OTAs) [9-11] and current conveyors [12-18], have been proposed due to commercial availabilities. The literature surveys show that a large number of modern circuit realizations for capacitance multipliers have been reported [10-18]. Unfortunately, these reported circuits suffer from one or more of the following weaknesses

- Need for passive element matching [9-11, 15-16].
- Lack of electronic tunability [12-15], [17], which can not be implemented in automatic control systems.
- Excessive use of the active and/or passive elements [10-18].
- Use of floating capacitor, which is not convenient to further fabricate in IC [9-11, 13, 17].
- Providing only a grounded capacitor, which offer applications less than a floating capacitor [11-13, 17].
- Use of a capacitor connected to inappropriate terminal, which results in an extra pole, and consequently lower frequency of operation [12, 18].

A major restriction of the all previous capacitance multipliers is temperature dependence of the capacitive values due to parasitic parameters of active elements used in circuits which limits the performances of the circuits, especially in the works suffered from environment variations.

Recently, a capacitance multiplier using DVCC and CCCIIIs has been introduced [19]. This circuit does not need any matching conditions of the elements. In addition, the capacitive value is ideally temperature-insensitive. Unfortunately, this reported circuit excessively uses active elements, which is not convenient to further fabricate in IC and provides high power consumption.

In this paper, we present a novel capacitance multiplier emphasizing on use of the DVCC and CCCCTA. The CCCCTA is an interesting active building block recently proposed [20], because it can be employ to synthesize and design the modern electronic circuits and systems employing only a few numbers of elements which subsequently offers low power consumption. The features of proposed circuit are that: the proposed circuits consume a two number of active element: it employs only single grounded capacitor, which is convenient to realize in IC [21-22]: it does not need any matching conditions of the employed elements: the capacitive value is temperature-insensitive. In addition, it can be controlled via input bias currents and offers low power
5. Conclusion
A novel floating capacitance multiplier using DVCC and CCCCTA has been introduced in this paper. The capacitive value can be widely adjusted by any input bias currents of the CCCCTA and is temperature-insensitive. The circuit construction comprises only two active elements, cooperating with a grounded capacitor. The PSPICE results confirm the mentioned features. The power consumption is approximately $321 \mu W$ at $\pm 1.5V$ supply voltages. Capacitance increasing and an application as a fifth-order Chebyshev high-pass filter were included to confirm usabilities of proposed capacitance multiplier. With the mentioned features, the proposed floating capacitance multiplier is consequently appropriate for further fabricating into an integrated circuit and implementing to capacitance-based circuits.

6. References


