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Single Element Based-Novel Temperature insensitive/Electronically Controllable Floating Capacitance Multiplier and Its Application

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Abstract- This article introduces floating capacitance multiplier using differential voltage current conveyor transconductance amplifiers (DV-CCTA). Its outstanding feature is that the capacitive value can be widely adjusted by input bias currents of the DV-CCTA and is theoretically temperature-insensitive. The circuit construction consists of only single DV-CCTA, with a grounded capacitor. The circuit performances are depicted through PSPICE simulations. They show good agreement to theoretical anticipation. Power consumption is approximately 0.48mW. Increasing capacitance and an application as a fourth-order Chebyshev high-pass filter are included to confirm the usability of the proposed circuit.

I. INTRODUCTION

It is well accepted that a capacitor is an important element which is frequently used in the most of circuits and systems. For example, it is used for tuning in filters, oscillators and etc. However, in the integrated circuit fabrication, it is impractical to realize large-valued capacitors because of the occupied area. In fact, in a standard CMOS polysilicon layers, a 20pF capacitor is equivalent, relatively to the silicon area, to thousands of transistors [1]. This means that the integration of capacitor as large as 100pF is not possible. In some applications, however, such as integrated lock-in amplifiers, sampled-data systems and capacitive sensor interfaces [2-5], they are necessary to have higher capacitive values.

A possible solution is the use of a capacitance multiplier, which performs the multiplication of small capacitive values, to obtain higher equivalent integrated capacitors, avoiding the need of a large silicon area [6]. From literature studies, several works which can provide a multiplied capacitor have been proposed. Although, the voltage-mode operational amplifier (op-amp) based capacitance multipliers are available in the literatures [7-9], they are not suitable from the view point of IC fabrication.

The modern active building blocks employ to synthesize the capacitance multipliers are emphasized on Operational Transconductance Amplifiers (OTAs) [9-11] and current conveyors [12-18] due to commercial availabilities. The literature surveys show that a large number of modern circuit realizations for capacitance multipliers have been reported [9-18]. Unfortunately, these reported circuits suffer from one or more of following weaknesses

- Need for passive element matching [9-11, 15-16].
- Lack of electronic tunability [12-15], [17], which cannot be implemented in automatic control systems.
- Excessive use of the active and/or passive elements [10-18].
- Use of floating capacitor, which is not convenient to further fabricate in IC [9-11, 13, 17].
- Use of a capacitor connected to in appropriate terminal, which results in an extra pole, and consequently lower frequency of operation [12, 18].

A major restriction of the all previous capacitance multipliers is temperature dependence of the capacitive values due to parasitic parameters of active elements used in circuits which limits the performances of the circuits, especially in the works suffered from environment variations.

Recently, the capacitance multipliers based on DVCC (differential voltage current conveyor) and CCCCTAs (current controlled current conveyors) [19], OTAs [20], DVCC cooperating with CCCCTA (current controlled current conveyor transconductance amplifier) [21] and CCCCTAs [22] have been introduced. These circuits do not need any matching conditions of the elements. In addition, the capacitive values are electronically adjustable and ideally temperature-insensitive. Unfortunately, the circuits in [19, 21] consist of many different active elements while the reported circuit in [20] comprises 4 OTAs and the reported circuit in [22] comprises 2 CCCCTAs. There can be found that the recently proposed topologies need to employ a lot of elements, which is not convenient to either further fabricate in IC or practically implement and providing higher power consumption.

In this paper, we present a novel capacitance multiplier emphasizing on use of the DV-CCTA, the DV-CCTA is an interesting active building block, because it can be employed to synthesize and design the modern electronic circuits and

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systems employing only a few numbers of elements. The obtained capacitive value can be widely adjusted by any input bias currents of the DV-CCTA and is temperature-insensitive. The circuit construction comprises only single DV-CCTA, cooperating with a grounded capacitor, which is suited to realize in IC [23-24]. The PSPICE simulation results confirm the mentioned features. Consequently, the proposed grounded capacitance multiplier is appropriate for and further fabricating into an integrated circuit and implementing to capacitance-based circuits. Capacitance increasing and an application as a fourth-order Chebyshev high-pass filter are included.

II. PRINCIPLE AND OPERATION

A. The Differential Voltage Current Conveyer Transconductance amplifier (DV-CCTA)

The DV-CCTA, whose electrical symbol and equivalent circuit are shown in Fig. 1, is a six-terminal network with the terminal ideal characteristics described by following equation

\[
\begin{bmatrix}
I_{Y1} \\
I_{Y2} \\
V_X \\
I_x \\
I_{01} \\
I_{02}
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 1 & -1 & 0 \\
1 & 0 & 0 & 0 \\
0 & 0 & 0 & \pm g_{m1} \\
0 & 0 & 0 & \pm g_{m2}
\end{bmatrix}
\begin{bmatrix}
I_X \\
V_{Y1} \\
V_{Y2} \\
V_x \\
V_z
\end{bmatrix},
\]  
(1)

where \(g_{m1}\) and \(g_{m2}\) are the transconductances of DV-CCTA. For a bipolar DV-CCTA, the transconductance gain can be expressed by

\[g_{m1} = \frac{I_{g1}}{2V_T},\]  
(2)

and

\[g_{m2} = \frac{I_{g2}}{2V_T},\]  
(3)

\(V_T\) is thermal voltage, it equals 26mV at a room temperature.

B. The proposed Floating Capacitance Multiplier

Fig. 2 depicts the proposed floating capacitance multiplier. Considering the circuit in Fig. 2 and using DV-CCTA properties in section II. A, we will receive

\[I_c = \frac{g_{m1}C_S}{g_{m2}}(V_1 - V_2),\]  
(4)

and

\[Z_m = \frac{(V_1 - V_2)}{I_c} = \frac{g_{m2}}{g_{m1}C_S},\]  
(5)

From Eq. (5), it is clearly seen that, the proposed circuit can provide the new floating capacitor with a value

\[C_{eq} = \frac{g_{m1}}{g_{m2}}C.\]  
(6)

Substituting the transconductance as shown in Eqs. (2)-(3) into Eq. (6), it will be changed to

\[C_{eq} = K_{mel}C = \frac{I_{g2}C}{I_{g1}},\]  
(7)

It is evident that, the capacitive value is multiplied with a gain

\[K_{mel} = \frac{I_{g1}}{I_{g2}}.\]  
(8)

It is found that, if the connected capacitor is free from temperature, the obtained capacitive value is temperature-insensitive and can be adjusted by any input bias currents.
Thus, $K_{\text{mul}}$ can be multiplied as high as more than 6 decades, because $I_{B1}$ can be as high as milliampere range, while $I_{B2}$ can be as low as nanoampere range.

**C. Analysis of non-ideal case**

For non-ideal case, the DV-CCTA can be respectively characterized with the following equation

$$
\begin{bmatrix}
I_{Y1} \\
I_{Y2} \\
V_X \\
I_z \\
I_{y1} \\
I_{y2}
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
\gamma & -\gamma & 0 & \gamma \\
\alpha & 0 & 0 & \gamma \\
0 & 0 & \pm \beta g_{m1} & \gamma \\
0 & 0 & \pm \beta g_{m2} & \gamma
\end{bmatrix}
\begin{bmatrix}
I_Z \\
V_{Y1} \\
V_{Y2} \\
V_Z \\
V_{y1} \\
V_{y2}
\end{bmatrix},
$$

(9)

$\alpha$ is the frequency dependent current gain besides $\beta$ and $\gamma$ are the frequency dependent voltage gains. These gains are ideally equal to unity. Practically, they depend on the frequency of operation, temperature and transistor parameters of the DV-CCTA.

In the case of non-ideal, an input impedance in Eq. (5) is converted to

$$
Z_{in} = \frac{V_C}{I_C} = \frac{\beta I_{B2}}{\alpha \gamma \beta I_{B3} s C}.
$$

(8)

Actually, the $\alpha$, $\beta$ and $\gamma$ originate from the intrinsic resistances and stray capacitances in the DV-CCTA. These errors affect the sensitivity to temperature and the high frequency response of the proposed circuit, then the DV-CCTA should be carefully designed to minimize these errors. Consequently, these deviations are very small and can be ignored in ideal consideration.

**D. Principle of capacitance increasing**

Fig. 3 depicts the possible implementation of the high-value capacitance controllabilities [19]. The output stage of circuit in Fig. 2 is constituted by current amplifier. Then, the output current of current amplifier are equal to $I_{O2} = n I_{in}$, where $n$ is the current gain of the current amplifier. So, the input impedance of circuit in Fig. 3 becomes

$$
Z_{in} = \frac{V_C}{I_C} = \frac{I_{B2}}{n I_{B3} s C}.
$$

(9)

It is evident that, the capacitive value is multiplied with a gain

$$
K_{\text{mul}} = \frac{n I_{B1}}{I_{B2}}.
$$

(10)

From Eq. (10), it is clearly seen that, we can also control the capacitive value by adjusting the current gain of the current amplifier.
III. SIMULATION RESULTS AND DISCUSSION

To prove the performances of the proposed circuit, the PSPICE simulation program was used for the examination. The PNP and NPN transistors employed in the proposed topology were simulated by respectively using the parameters of the PR200N and NR200N bipolar transistors of ALA400 transistor array from AT&T [25]. The DV-CCTA employed in the proposed circuit was simulated with ±1.5V supply voltages. Fig. 4 depicts schematic descriptions of the DV-CCTA used in the simulations.

To illustrate frequency response of the floating capacitance multiplier, Fig. 5 shows the absolute magnitude of input impedance for several frequencies. It should be noted that the usable frequency range of the proposed circuit is up to approximately 2MHz. At higher frequencies, the internal parasitic elements, covering capacitances and resistances, degrade the performances of the proposed circuit. Similarly, these factors effect on temperature dependence of input impedance at the higher frequencies, as shown in Fig. 6.

In addition, from the result in Fig. 6, it is insisted that in the usable frequency range, the proposed circuit provides a floating capacitance with temperature-insensitivities. Fig. 7 shows the absolute magnitude of input impedances relative to frequency variations for different n of circuit in Fig. 3, where n is the current gain of the ideal current amplifier used for the simulation.

To show usability of the proposed circuit, an application as a fourth-order Chebyshev high-pass filter as shown in Fig. 8 is included. The results of frequency responses of the proposed capacitance multiplier, compared to the ideal capacitance, are confirmed in Fig. 9, where $V_{in}=1$mV.

The results of the capacitance deviations due to temperature variations are about -0.52% at 0°C and 0.55% at 100°C, as shown in Fig. 10.

Table 1 displays capacitance deviations of obtained capacitances due to capacitance and multiplied gain variations. It is seen that the simulation results are in accordance with the theoretical analysis as shown in Eq. (10).
A novel floating capacitance multiplier with temperature insensitive/electronically controllable employing only single DV-CCTA has been introduced in this paper. The capacitive value can be widely adjusted by any input bias currents of the DV-CCTA and is slightly temperature independent. The circuit construction is composed of only single active elements, cooperating with a grounded capacitor. The PSPICE circuit construction is composed of only single active elements, cooperating with a grounded capacitor. The PROSIC results confirm the mentioned features. The power consumption is approximately 0.48mW at ±1.5V supply voltages. Consequently, the proposed floating capacitance multiplier is appropriate for further fabricating into an integrated circuit and subsequently implementing to capacitance-based circuits. Capacitance increasing and an application as a fourth-order Chebyshev high-pass filter are included, they show good performances of the proposed capacitance multiplier.

### IV. CONCLUSION

REFERENCES


